Amendment to the Claims:

This listing of claims will replace all versions, and listings, of claims in the application:

Listing of Claims:

1 – 8 (Cancelled).

9. (Original) A spread spectrum clock generator comprising:

means adapted for receiving a periodic clock signal having a generally constant frequency;

a frequency divider for generating a lower frequency clock signal from a received periodic clock signal;

a programmable digital delay line adapted to receive the lower frequency clock signal, and including means provide a selected delay to the lower frequency clock signal in accordance with a received digital delay value so as to form a varying frequency clock signal;

a counter for generating a preselected digital sequence;

a pattern generator adapted for generating the digital delay value in accordance with the preselected digital sequence;

a frequency multiplier for increasing a frequency of the varying frequency clock signal so as to generate a spread spectrum clock signal; and

means adapted for communicating the spread spectrum clock signal to an associated digital device.

10. (Original) The spread spectrum clock generator of claim 10 wherein the spread spectrum clock signal has a frequency range between $1/(T-4\Delta)$ and $1/(T+4\Delta)$, wherein T is defined as a period of the clock input signal and Δ is defined as the selected delay.

11. (Original) The spread spectrum clock generator of claim 10 wherein the frequency range of the spread spectrum clock signal linearly alternates between $1/(T-4\Delta)$ and $1/(T+4\Delta)$.

12. (Original) The spread spectrum clock generator of claim 11 wherein the frequency range of the spread spectrum clock signal varies from -.2% to +.2% of the periodic clock signal.

13. (Currently Amended) The spread spectrum clock generator of claim 12 wherein the pattern generator includes ~~means for generating~~ a digital delay value generator to output the digital delay value in accordance with values disposed in a preselected truth table.

14. (Currently Amended) The spread spectrum clock generator of claim 11 wherein the counter operates ~~synchronously~~ in response to with the periodic clock signal.

15 – 20 (Cancelled).

21. (New) A spread spectrum clock generator comprising:

a clock input adapted for receiving a clock signal having a generally constant frequency;

a digital delay having,

delay input adapted for receiving the clock signal from the clock input and a clock output,

data input adapted for receiving delay data representative of a selected delay, and

a clock output, the clock output adapted to communicate a modified clock signal, the frequency of the modified clock signal is adjusted in accordance with the delay data;

a numeric sequencer adapted for generating a selected numeric output data representative of a selected numeric sequence; and

means for communicating the numeric output data to the data input as the delay data;

wherein the numeric sequencer includes a binary counter for generating a binary output sequence;

wherein the numeric sequencer further includes a pattern generator, which pattern generator receives the binary output sequence from the binary counter, and generates the delay data as a function of the binary output sequence;

wherein the modified clock signal has a frequency range between $1/(T-4\Delta)$ and $1/(T+4\Delta)$, wherein T is defined as a period of the clock input signal and Δ is defined as the selected delay.

22. (New) The spread spectrum clock generator of claim 21 wherein the frequency range of the modified clock signal linearly alternates between $1/(T-4\Delta)$ and $1/(T+4\Delta)$.

23. (New) The spread spectrum clock generator of claim 22 further comprising a signal conditioner adapted for receiving the modified clock signal and generating a conditioned clock signal therefrom.

24. (New) The spread spectrum clock generator of claim 23 wherein the signal conditioner further comprises a frequency multiplier.

25. (New) The spread spectrum clock generator of claim 24 wherein the signal conditioner includes a phase lock loop.

26. (New) A method of generating a spread spectrum clock signal comprising the steps of:

receiving a clock signal having a generally constant frequency;

generating a low frequency clock signal corresponding to the received clock signal;

generating selected numeric output data representative of a selected numeric sequence, which numeric output data is generated synchronously with the received clock signal;

generating a varying frequency clock signal from the low frequency clock signal, the delayed clock signal having a delay set in accordance with the selected numeric output sequence;

increasing the overall frequency of the varying frequency clock signal;

wherein the step of generating selected numeric output data includes the steps of:

incrementing a counter in accordance with the received clock signal;

generating counter data representative of a state of the counter;

generating pattern data that corresponds to the counter data; and

generating the selected numeric sequence from the pattern data;

wherein the step of generating pattern data includes the step of generating the spread spectrum clock signal in accordance with values associated with a preselected truth table.

27. (New) The method of generating a spread spectrum clock signal of claim 26 wherein the spread spectrum clock signal has a frequency range between $1/(T-4\Delta)$ and $1/(T+4\Delta)$, wherein T is defined as a period of the clock input signal and Δ is defined as the selected delay.

28. (New) The method of generating a spread spectrum clock signal of claim 27 wherein the frequency range of the spread spectrum clock signal linearly alternates between $1/(T-4\Delta)$ and $1/(T+4\Delta)$.

29. (New) The method of generating a spread spectrum clock signal of claim 28 wherein the frequency range of the spread spectrum clock signal varies from -.2% to +.2% of the periodic clock signal.